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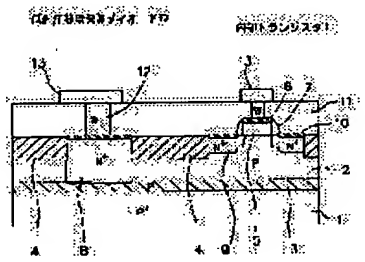
(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device provided with an electrostatic protective element in which characteristics of a MOS transistor is prevented from fluctuating, etc., due to static electricity discharge.

SOLUTION: A heavily doped PN junction is formed between a heavily doped N+ cathode region 8 and a boron-protruded region 3 on a P+ substrate 1, and a low voltage-proof diode D breaking down at low reverse voltage is formed. By using it as an electrostatic protective element of an input circuit or an output circuit, an internal element transistor is effectively protected from an application surge even when a gate oxide film is made thin.



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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by making hard flow connection between the gate electrode of said MOS transistor, or a drain field and a high concentration semi-conductor substrate, and having diode with the high impurity concentration higher than the high impurity concentration by the side of the anode in the drain plane of composition of said MOS transistor by the side of the anode in the plane of composition as a static protection component of said MOS transistor in the semiconductor device with which an MOS transistor is formed on the semi-conductor layer of the 1st conductivity type by which epitaxial growth was carried out on the high concentration semi-conductor substrate of the 1st conductivity type.
[Claim 2] The semiconductor device according to claim 1 with which hard flow pressure-proofing of the diode which is said static protection component is characterized by being lower than drain junction pressure-proofing of said MOS transistor.
[Claim 3] The semiconductor device according to claim 1 with which hard flow pressure-proofing of the diode which is said static protection component is characterized also for the proof-pressure twist of the gate oxide of said MOS transistor by the low thing.
[Claim 4] The semiconductor device according to claim 1 or 2 characterized by the plane of composition of the diode which is said static protection component existing in the place near [plane of composition / of said MOS transistor / drain] said high concentration semi-conductor substrate.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the semiconductor device which has a static protection component in the silicon LSI using an epitaxial substrate about a semiconductor device.
[0002]
[Description of the Prior Art] In a semiconductor device, when the rated value it is supposed that must not be used more than that specified value exists and it is used exceeding this rated value, the property of a semiconductor device changes or it is destroyed. However, the so-called surge which is a sudden electric pulse exceeding the rated value may be impressed to a semiconductor device.
[0003] Then, various approaches are proposed in order to protect a semiconductor device from this surge. About the Prior art for protecting a semiconductor device from this surge, they are Anant.G.Sabnis work and "BUIERU S eye electronics. Micro structure Science It explains below using Vol.22(VLSI ELECTRONICS MICROSTRUCTURE SCIENCE Vol.22)."
[0004] According to this conventional technique, the internal transistor of LSI is protected from the surge impressed to an external terminal by the static protection component. As shown in (a) of drawing 8 , in order to impress a surge to the gate oxide of a direct internal circuitry, to change the property of a transistor or to prevent in MOSLSI that gate oxide is destroyed, the protection component is prepared in the input terminal. That is, diodes 81 and 82 are connected with an external terminal between GND between an external terminal and VDD, respectively, and it is serving to ease the stress to the gate oxide of an internal transistor by making the charge generated by impression of a surge discharge through such diodes. On the other hand, about an output terminal, drain junction of the output transistor T80 plays the role of a protection component.
[0005] Moreover, as shown in (b) of drawing 8 , by the logic LSI represented by the gate array, the gate control mold diodes 83 and 84 with a protective effect higher than diode are used as a protection component of an input terminal. The gate control mold diodes 83 and 84 used the MOS transistor, the NMOS mold 84 is connected to GND and the PMOS mold 83 has connected the gate terminal for control to VDD. Although the property of the forward direction is equivalent to the above-mentioned diode, since the property of hard flow is broken down on an electrical potential difference (BVds) lower than the above-mentioned diode, the protective effect over a surge increases. Furthermore, in the NMOS mold 84, since a protection component turns on on a still lower electrical potential difference using a snapback phenomenon by connecting a source terminal to GND and considering as metal-oxide-semiconductor structure, the protective effect over a surge has been heightened further.
[0006] On the other hand, although thin-film-izing of gate oxide is indispensable to improvement in the speed of LSI, and high integration, in connection with it, the surge resistance of gate oxide becomes weak. However, the protection components 83 and 84 mentioned above are all metal-oxide-semiconductor structures, and had the trouble of a surge being impressed to the gate oxide of a protection component, and leakage current having increased or becoming easy to result in destruction. Furthermore, with the output transistor T80 which serves as the role of a protection component, even if

it did not result in destruction, it had the trouble of doing effect to circuit actuation, by property fluctuation by charge being poured into gate oxide.

[0007] As an approach of solving the above-mentioned trouble, it is Y.Fong and C.Hu. Work "internal IESUDE The structure which added the field transistor to the conventional protection component is used as shown in tolan JIENTSU Inn input protection sir KITTSU (Internal ESD Transients in Input Protection Circuits IEEE/IRPS 1989)." As shown in (a) of drawing 9 , the field transistor (Thick Field Device, TFD) 90 is inserted between the conventional protection components (Field Plate Diode, FPD) 91 and 92 and the input pads 93 which were mentioned above. To an output transistor, as shown in (b) of drawing 9 , the field transistor (TFD) 95 is inserted between two output transistors of the PMOS mold 96 and the NMOS mold 97, and output pads 98.

[0008] Next, the cross-section structure of the conventional field transistor is shown in drawing 10 . This transistor is adjoining N+ separated with the isolation oxide film 4. It is the parasitism bipolar transistor which uses the diffusion layer field 31 as an emitter and a collector, and uses P wells 2 as the base, and the electrode for control which covers the isolation oxide film 4 is connected to the collector. N+ The diffusion layer field 31 is formed in the source field and the drain field, and coincidence of an NMOS transistor, and an NMOS transistor is formed on P wells 2. N+ The metal silicide 10 for attaining low resistance-ization is formed in the diffusion layer field 31 or the front face of the gate electrode 6 of an MOS transistor. here — 5 — gate oxide and 6 — for an N+SD field and 11, as for an embedding electrode and 13, a substrate interlayer insulation film and 12 are [a gate electrode and 7 / a side-attachment-wall oxide film and 9 / a wiring electrode and 30] P type substrates.

[0009] Next, the protective effect over the surge of the conventional semiconductor device is explained with reference to drawing 9 and drawing 10 . When forward surge voltage is impressed to the input pad 93 shown in drawing 9 , or the output pad 98, the parasitism bipolar transistor between collector emitters was made to turn on, and the protection component and the output transistors 96 and 97 of the next step are protected by missing a surge. negative electrical-potential-difference impression — receiving — Collector P — a well — since the diode of a between serves as a forward bias — the bias more than Vf — receiving — P — charge can be missed to a well 2.

[0010] Therefore, with the static protection component using this conventional field transistor, the gate oxide of an internal circuitry or gate control mold diode is protected from the surge by making a field transistor turn on.

[0011]

[Problem(s) to be Solved by the Invention] However, the protective effect of a semiconductor device is still inadequate, and amplification of the effectiveness is demanded. in order to increase the protective effect in the conventional semiconductor device — the increase of area and the charge accompanying [carry out and] a surge of a field transistor — a sink — easy — the approach of carry out — or although there is the approach of make it into the device structure which a transistor tends to turn on, it not only opposes towards detailed-izing of LSI, but the effect on the circuit property accompanying the increment in parasitic capacitance is large, and there is a trouble of a margin of operation decrease about the former. It is necessary to low-concentration-ize P wells 2 first, and to raise the injection efficiency of the carrier from an emitter to the base about the latter.

[0012] However, for detailed-izing of LSI, high concentration-ization of a well becomes indispensable so that it may be represented by the scaling law. Moreover, it is the technique made indispensable also in order for high concentration-ization of a well to realize detailed isolation, therefore low-concentration-izing P wells and raising the injection efficiency of the carrier from an emitter to the base disagrees with the function needed for a field transistor. the production process of a field transistor — setting — PR (photoresist) process — adding — the impurity of N type — P — carrying out an ion implantation to a well — P of the field transistor formation section — although it is also possible only for a well to lower effective high impurity concentration, by this approach, it has the trouble of an ion implantation that the manufacture variation of the concentration control depended for striking back is very large.

[0013] Moreover, from 0.25-micrometer process order, in order to realize detailed isolation, a shallow trench separation (STI) technique is used. In the component isolation construction by the shallow trench, since a separation oxide film's being thick and the configuration of the side face become near vertically, it has the trouble of being hard coming to turn on a field transistor.
[0014] Therefore, with the static protection component using the conventional field transistor, it is difficult with improvement in the speed of LSI, and detailed-izing to heighten a protective effect. On the other hand, if the gate oxide of an MOS transistor is thin-film-ized, the resistance over charge impregnation of gate oxide will become weak. Therefore, it is faced with the trouble of becoming easy for the dependability of gate oxide to fall, by the ESD (ElectroStatic Discharge) damage.
[0015] It aims at offering the semiconductor device which this invention was made in view of the above-mentioned situation, realizes a reliable integrated circuit device, reduces the size of an input output buffer, and can be contributed also to high integration of LSI and which has the static protection component of the high structure of a protective effect to ESD.
[0016]
[Means for Solving the Problem] In the semiconductor device with which an MOS transistor is formed on the semi-conductor layer of the 1st conductivity type with which epitaxial growth of the invention according to claim 1 was carried out on the high concentration semi-conductor substrate of the 1st conductivity type As a static protection component of said MOS transistor, hard flow connection is made between the gate electrode of said MOS transistor, or a drain field and a high concentration semi-conductor substrate. And it is characterized by having diode with the high impurity concentration higher than the high impurity concentration by the side of the anode in the drain plane of composition of said MOS transistor by the side of the anode in the plane of composition.
[0017] Hard flow pressure-proofing of the diode whose invention according to claim 2 is said static protection component in invention according to claim 1 is characterized by being lower than drain junction pressure-proofing of said MOS transistor.
[0018] Hard flow pressure-proofing of the diode whose invention according to claim 3 is said static protection component in invention according to claim 1 is characterized by the proof-pressure twist of the gate oxide of said MOS transistor being low.
[0019] Invention according to claim 4 is characterized by the plane of composition of the diode which is said static protection component existing in the place near [plane of composition / of said MOS transistor / drain] said high concentration semi-conductor substrate in invention according to claim 1 or 2.
[0020] therefore, the thing for which a breakdown current is passed to the electrical potential difference more than junction pressure-proofing of diode in the semiconductor device concerning this invention when forward surge voltage is impressed from an external terminal -- diode — letting it pass — charge — low — it can miss to a substrate [****]. On the other hand, since the forward bias of the diode is carried out to negative surge voltage, charge can be missed to a substrate by passing forward current to the electrical potential difference more than Vf.
[0021] thus, the surge impressed from the outside -- receiving — diode — letting it pass — efficient — charge — low — by missing to a substrate [****], it is impressed to an MOS transistor, and gate oxide is made to destroy or charge serves to prevent causing property fluctuation.
[0022]
[Embodiment of the Invention] Next, 1 operation gestalt of the semiconductor device concerning this invention is explained with reference to a drawing. Drawing 1 is the sectional view of the 1st operation gestalt of the low proof-pressure static protection diode D and the semiconductor device concerning this invention which has the internal transistor T. However, the same number is given to the same member as the conventional semiconductor device shown in drawing 10. This semiconductor device is P+. P wells 2 are formed through the boron **** riser field 3 on the mold substrate 1, and it is N+. The low proof-pressure static protection diode D is formed between the cathode field 8 and the boron ****

riser field 3, and the internal transistor T (the inside of drawing NMOS transistor) is formed on P wells 2. Moreover, N+ The metal silicide 10 for attaining low resistance-ization is formed in the front face of the cathode field 8, the N+SD field 9, and the gate electrode 6. Although Co silicide is used in the operation gestalt described below as this metal silicide, since this metal silicide attains low resistance-ization, it is not used, and this invention may not be limited to Co silicide and may use suitable metal silicide. Junction pressure-proofing of the low proof-pressure static protection diode D is higher than the supply voltage of LSI, and is set up lower than gate pressure-proofing of the internal transistor T.

[0023] Drawing 2 is the sectional view showing the production process of the semiconductor device shown in drawing 1 . First, P+ P wells 2 are formed through the boron **** riser field 3 on the mold substrate 1. Specifically, it is P-/P+. P wells 2 are formed by the ion implantation on a substrate. And the isolation oxide film 4 is formed selectively ((a) of drawing 2). Next, it is N+ by carrying out the ion implantation of the N type impurity ion by using a photoresist (PR) 20 as a mask. The cathode field 8 is formed ((b) of drawing 2).

[0024] Next, etching which uses the mask material 21 as a mask performs patterning of the gate electrode 6 of an internal transistor after forming gate oxide 5 ((c) of drawing 2). Then, the source drain field of the transistor of LDD structure is formed with a well-known technique using the side-attachment-wall oxide film 7. At this time, the ion implantation for forming the N+SD field 9 is N+. It also gives a cathode field ((d) of drawing 2). Then, with a well-known technique, metal silicide 10 is formed on the surface of silicon, the formation of the substrate interlayer insulation film 11, puncturing of a contact field, the formation of an implanted electrode 12, the formation of the wiring electrode 13, and patterning which are shown in drawing 1 are performed, and the semiconductor device of the structure shown in drawing 1 is completed.

[0025] Drawing 3 and drawing 4 are drawings showing 1 operation gestalt of the I/O circuit using the semiconductor device which has the structure shown in drawing 1 .

[0026] Drawing 3 is drawing showing an input-protection circuit, and the low proof-pressure static protection diode 35 and the gate control mold diodes 36 and 37 are connected between the input terminal and the internal circuitry. A cathode is connected to an input terminal and, as for the low proof-pressure static protection diode 35, an anode is connected to GND. Furthermore, from a cathode, it connects with the gate control mold diodes 36 and 37 of two molds, N type and P type, through resistance 38. These two gate control mold diodes 36 and 37 are protection components currently used from the former, and are further connected to an internal circuitry through resistance 39.

[0027] Drawing 4 is drawing showing an output protection network, and the low proof-pressure static protection diode 40 is formed between the output transistors T40 and T41 and an output terminal. A cathode is connected to the drain of the output transistors T40 and T41, and the anode is connected to GND.

[0028] Drawing 5 shows the example of arrangement of the low proof-pressure static protection component in the chip of LSI. an input/output terminal (PAD) 50 — immediately, inside the low proof-pressure static protection diode formation field 51 is formed, and the low proof-pressure static protection diode of all input output buffers is formed in this field. And the inside enclosed in this low proof-pressure static protection diode formation field 51 serves as the internal area 52. In the case of an input buffer, the gate control mold diode and the internal circuitry which are shown in drawing 3 are arranged, and the internal circuitry containing the output transistor shown in the field sign 4 which is an output buffer is arranged in the internal area 52.

[0029] Next, the protected operation to the surge of the semiconductor device concerning the 1st operation gestalt is further explained to a detail with reference to drawing 3 and drawing 4 . In the input-protection circuit shown in drawing 3 , if a surge is impressed to an input terminal, the gate control mold diodes 36 and 37 will be protected from an impression surge by the low proof-pressure static protection diode 35, and an internal circuitry will be further protected by work of the low proof-pressure static protection diode 35 and the gate control mold diodes 36 and 37. that is, the case where forward surge

voltage is impressed — the electrical potential difference more than the junction pressure-proofing between cathode-anodes — receiving — a junction breakdown current — the low proof-pressure static protection diode 35 — letting it pass — low — P+ [****] Charge can be missed to a mold substrate.
[0030] Since the hard flow junction pressure-proofing between the cathode-anodes of the low proof-pressure static protection diode 35 is set up lower than pressure-proofing of gate oxide, it can reduce the amount of charges poured into the gate oxide of the gate control mold diodes 36 and 37 from a side face. Thereby, the static protection capacity over the internal circuitry of the gate control mold diodes 36 and 37 changes, or it prevents destroying gate oxide. On the other hand, since the forward bias of the low proof-pressure static protection diode 35 is carried out to negative surge voltage, it is P+ at the electrical potential difference more than Vf. Charge can be missed to a mold substrate.
[0031] In the output circuit shown in drawing 4 , the output transistors T40 and T41 are protected from the surge impressed to the output terminal by the low proof-pressure static protection diode 40. About actuation of the low proof-pressure static protection diode 40, since it is the same as that of actuation of the low proof-pressure static protection diode 35 shown in above-mentioned drawing 3 , it omits.
[0032] Next, the structure of the 1st operation gestalt of the semiconductor device concerning this invention is further explained to a detail. P+ which contained boron 1x1019-1020cm-3 in the semiconductor device shown in drawing 1 On the mold substrate 1, P wells 2 whose surface boron concentration is about [one to 5x1017cm -] three are formed, and it is P+. The boron **** riser field 3 which contained boron 1x1018-1019cm-3 exists between the mold substrate 1 and P wells 2. The thickness of about 1.5 micrometers and P wells 2 of the thickness of the boron **** riser field 3 is about 1 micrometer.
[0033] Moreover, N+ which contained the N type impurity 1x1018-1020cm-3 It is prepared so that the cathode field 8 may touch the boron **** riser field 3. Here, the high impurity concentration of N+ cathode field 8 in a plane of composition is set about [5x1019cm -] to three. N+ The low proof-pressure static protection diode D is formed between the cathode field 8 and the boron **** riser field 3, and the hard flow pressure-proofing is about 4V. On the other hand, on P wells 2, the internal transistor (NMOS transistor) T of LDD structure is formed. Moreover, the thickness of gate oxide 5 is about 5nm. N+ In order to attain low resistance-ization, metal silicide (Co silicide) 10 is formed in the front face of the cathode field 8, the N+SD field 9 of an MOS transistor, and the gate electrode 6.
[0034] Next, with reference to the sectional view of the production process of the semiconductor device shown in drawing 2 , the semiconductor device concerning this invention is further explained to a detail. P+ which contained boron 1x1019-1020cm-3 About 2.5 micrometers of silicon containing about [1x1015cm -] three boron are grown up on the mold substrate 1. At this time, it is P+. The boron **** riser field 3 which 1x1018-1019cm-3 </SUP> Contained boron by the autodoping and thermal diffusion from the mold substrate 1 is formed in the thickness which is about 1.5 micrometers. Then, the isolation oxide film 4 which consists of silicon oxide with a thickness of about 400nm with a well-known technique is formed. and the field in which an NMOS transistor and low proof-pressure static protection diode are formed after preparing an oxide film (un-illustrating) with a thickness of about 20nm in a front face — the ion implantation of boron — giving — P — a well 2 is formed ((a) of drawing 2).
[0035] This ion implantation is performed 3 times on condition that the acceleration voltage of 300kV, 3x1013cm [of douse] - 2 and acceleration voltage of 150kV, 5x1012cm [of douse] - 2 and acceleration voltage of 30kV, and douse 5x1012cm-2. It carries out for accumulating, and the 2nd impregnation performs 3rd impregnation in order [of punch-through prevention of the isolation between NMOS transistors, and an NMOS transistor] to obtain desired Vt. Then, the ion implantation of the impurity of N type is carried out to the field which forms a PMOS transistor, and a field is formed in it N well (un-illustrating). Then, it is N+ by performing patterning of a photoresist 20 and pouring in Lynn by using a photoresist 20 as a mask. The cathode field 8 is formed ((b) of drawing 2).
[0036] Lynn impregnation is performed 3 times on condition that the acceleration voltage of 1MV, 5x1014 to 1x1015cm [of douse] - 2 and acceleration voltage of 300kV, 5x1014cm [of douse] - 2 and

acceleration voltage of 70kV, and douse 1x1014cm-2. Performing the first impregnation in order to opt for junction pressure-proofing of low proof-pressure static protection diode, the 2nd time and the 3rd impregnation are N+. It carries out in order to pull out the cathode field 8 to low resistance to a silicon front face. Then, crystalline recovery and the redistribution of an impurity are given by the 850 degrees C - 900 degrees C drive-in. Then, with a well-known technique, after forming gate oxide 5 with a thickness of 5nm, the gate electrode which consists of silicon with a thickness of about 200nm is formed in the whole surface.

[0037] And the gate electrode 6 of an MOS transistor is processed by etching which uses as a mask the mask material 21 by which patterning was carried out ((c) of drawing 2). The gate length of an internal transistor processes about 0.15 micrometers. Then, the source drain field of the transistor of LDD structure is formed with a well-known technique using the side-attachment-wall oxide film 7. For example, after carrying out the ion implantation of the arsenic to an NMOS transistor on condition that the acceleration voltage of 20kV, and dose 2x1013cm-2, etchback of the about 60nm oxide film is grown up and carried out to the whole surface. Thereby, the side-attachment-wall oxide film 7 is formed. Then, the ion implantation of an arsenic is performed to the field containing an NMOS transistor and low proof-pressure static protection diode, and the N+SD field 9 is formed in it ((d) of drawing 2).

[0038] The ion implantation of an arsenic is performed the acceleration voltage of 40kV, and in dose 1-5x1015cm-2. Then, the P+SD field (un-illustrating) of a PMOS transistor is formed by the ion implantation of boron. This ion implantation is performed by the acceleration voltage of about 10kV, and dose 1-5x1015cm-2. Then, the semiconductor device which has the structure shown in drawing 1 is completed by forming metal silicide (Co silicide) 10 with a thickness of about 20nm on the surface of silicon, and performing formation of the substrate interlayer insulation film 11 with a thickness of about 0.8 micrometers, puncturing of a contact field, formation of the implanted electrode 12 of W, formation of the wiring electrode 13 which consists of AlCu, and patterning with a well-known technique.

[0039] therefore, the thing for which a breakdown current is passed to the electrical potential difference more than junction pressure-proofing of diode according to this 1st operation gestalt — Diode D — letting it pass — charge — low — P+ [****] It can miss to the mold substrate 1. It is charge by on the other hand, passing forward current to the electrical potential difference more than Vf, since the forward bias of the diode D is carried out to negative surge voltage P+ It can miss to the mold substrate 1.

[0040] Next, the 2nd operation gestalt of the semiconductor device concerning this invention is explained with reference to a drawing. Drawing 6 is the sectional view of the 2nd operation gestalt of the semiconductor device concerning this invention which has the low proof-pressure static protection diode D and the internal transistor T as a static protection component. However, the same number is given to the same member as the semiconductor device concerning the 1st operation gestalt shown in drawing 1 . This semiconductor device is P+. P wells 2 are formed through the boron **** riser field 3 on the mold substrate 1.

[0041] moreover, P — the inside of a well 2 — P+ the anode field 14 prepares — having — N+ The cathode field 8 and P+ the low proof-pressure static protection diode D forms between the anode fields 14 — having — P — the internal transistor T (all over drawing, formed as an NMOS transistor.) is formed on the well 2. N+ The metal silicide 10 for attaining low resistance-ization is formed in the front face of the cathode field 8, the N+SD field 9, and the gate electrode 6. Moreover, junction pressure-proofing of the low proof-pressure static protection diode D is higher than the supply voltage of LSI, and the gate proof-pressure twist of the internal transistor T is set up low.

[0042] Drawing 7 is the sectional view showing the production process of the semiconductor device shown in drawing 6 . It is P+ like the 1st operation gestalt. After forming P wells 2 through the boron **** riser field 3 on the mold substrate 1, formation of gate oxide 5 and etching which uses the mask material 21 as a mask perform patterning of the gate electrode 6 of an internal transistor ((a) of drawing 7). Then, the source drain field of the transistor of LDD structure is formed with a well-known

technique using the side-attachment-wall oxide film 7. It is P+ by the ion implantation of the boron which uses a photoresist 23 as a mask after forming the N type LDD field 22 and the side-attachment-wall oxide film 7. The anode field 14 is formed ((b) of drawing 7).

[0043] And the ion implantation of the arsenic for forming the N+SD field 9 is performed also to a low proof-pressure static protection diode field, and it is N+. The cathode field 8 is formed ((c) of drawing 7). Then, with a well-known technique, metal silicide 10 is formed on the surface of silicon, formation of the substrate interlayer insulation film 11, puncturing of a contact field, formation of an implanted electrode 12, formation of the wiring electrode 13, and patterning are performed, and the semiconductor device of the structure shown in drawing 6 is completed.

[0044] Therefore, even if it uses the semiconductor device which is this 2nd operation gestalt, possible [constituting an I/O circuit as shown in drawing 3 - drawing 5] therefore, the same actuation as the 1st operation gestalt can be realized, and the same effectiveness as the 1st operation gestalt can be acquired.

[0045] Next, the structure of the 2nd operation gestalt of the semiconductor device concerning this invention is further explained to a detail with reference to drawing 6 and drawing 7 . When drawing 6 is referred to, this semiconductor device is P+. P wells 2 are formed on the mold substrate 1, and it is P+. The boron **** riser field 3 exists between the mold substrate 1 and P wells 2. The high impurity concentration and thickness of each field are good as almost the same as the high impurity concentration and thickness in the 1st operation gestalt shown in drawing 1 . Moreover, P+ which contained the P type impurity 1x1018-1019cm-3 It is prepared so that the anode field 14 may touch the boron **** riser field 3, and it is P+. N+ which contained the arsenic 1x1020-1021cm-3 all over the anode field 14 The cathode field 8 is formed.

[0046] N+ The cathode field 8 and P+ The low proof-pressure static protection diode D is formed between the anode fields 14, and the hard flow pressure-proofing is about 4V. On the other hand, on P wells 2, the internal transistor (NMOS transistor) T of LDD structure is formed. Furthermore, the thickness of gate oxide 5 is about 5nm. N+ In order to attain low resistance-ization, metal silicide (Co silicide) 10 is formed in the cathode field 8, the N+SD field 9 of an MOS transistor, and the front face of the gate electrode 6.

[0047] Next, with reference to production process drawing of the semiconductor device concerning the 2nd operation gestalt shown in drawing 7 , the semiconductor device concerning the 2nd operation gestalt is further explained to a detail. however, the production process of the semiconductor device concerning the 1st operation gestalt shown in drawing 2 — the same — P+ the isolation oxide film 4 which consists of silicon oxide after growing up silicon on the mold substrate 1 — forming — P — a well 2 and N which is not illustrated — a well is prepared. The conditions of a process are the same as the 1st operation gestalt. Then, crystalline recovery and the redistribution of an impurity are given by the 850 degrees C - 900 degrees C drive-in. Furthermore, with a well-known technique, after forming gate oxide 5 with a thickness of 5nm, the gate electrode 6 which consists of silicon with a thickness of about 200nm is formed in the whole surface. And the gate electrode 6 of an MOS transistor is processed by etching which uses as a mask the mask material 21 by which patterning was carried out ((a) of drawing 7). The gate length of an internal transistor processes about 0.15 micrometers.

[0048] Then, the source drain field of the transistor of LDD structure is formed with a well-known technique using the side-attachment-wall oxide film 7. For example, after carrying out the ion implantation of the arsenic to an NMOS transistor on condition that the acceleration voltage of 20kV, and dose 2x1013cm-2, etchback of the about 60nm oxide film is grown up and carried out to the whole surface. Thereby, the side-attachment-wall oxide film 7 is formed. Then, it is P+ to the field which forms low proof-pressure static protection diode by the ion implantation of the boron which uses a photoresist 23 as a mask. The anode field 14 is formed ((b) of drawing 7). The ion implantation of boron is performed on condition that - with acceleration voltage [of 300kV], and a dose of 5x1014cm 2 and acceleration voltage of 120kV, and dose 1-5x1014cm-2 ((c) of drawing 7).

[0049] Then, crystalline recovery and the redistribution of an impurity are given by the 850-900-degree C drive-in. Furthermore, the ion implantation of an arsenic is performed to the field containing an NMOS transistor and low proof-pressure static protection diode, and they are the N+SD field 9 and N+. The cathode field 8 is formed ((c) of drawing 7). An ion implantation is performed the acceleration voltage of 40kV, and in dose 1-5x1015cm-2. Then, the P+SD field (un-illustrating) of a PMOS transistor is formed by the ion implantation of boron.
[0050] The ion implantation of this boron is performed by the acceleration voltage of about 10kV, and dose 1-5x1015cm-2. Then, with a well-known technique, metal silicide (Co silicide) 10 with a thickness of about 20nm is formed on the surface of silicon, formation of the substrate interlayer insulation film 11 with a thickness of about 0.8 micrometers, puncturing of a contact field, formation of the implanted electrode 12 shown by W, formation of the wiring electrode 13 which consists of AlCu, and patterning are performed, and the semiconductor device which has the structure of drawing 6 is completed.
[0051] In this 2nd operation gestalt, since the **** riser of boron is not used like the 1st above-mentioned operation gestalt but the high concentration anode field 14 is formed by the ion implantation while the same effectiveness as the 1st above-mentioned operation gestalt is acquired, it is possible for control of concentration to become easy and to make small manufacture variation of pressure-proofing of low proof-pressure static protection diode.
[0052]
[Effect of the Invention] Since diode which consists of a high-concentration PN junction is used as the static protection component according to this invention so that clearly from the above explanation, hard flow junction pressure-proofing can be set up low, it becomes possible to the impression surge of hard flow to miss charge to a silicon substrate through diode efficiently, and an internal component can be protected. Therefore, since the static protection function to the MOS transistor made detailed can be improved, a reliable semiconductor device can be offered.
[0053] For example, if the case where the thickness of the gate oxide of an MOS transistor is 5nm is assumed and the electrical-potential-difference stress beyond 5V will be impressed to gate oxide, property fluctuation will become remarkable, and if impression time amount becomes long, it will result in destruction of gate oxide. An assumption of actuation by supply voltage 2.5V requires the protection component which is in an OFF state and goes into an ON state on the electrical potential difference not more than 5V in impression of 2.5V. Such a protection component is easily realizable with the structure of the protection diode which the semiconductor device applied to this invention to implementation having been difficult for with the conventional protection component has. Furthermore, it becomes possible to form diode which causes a hard flow breakdown by 4V by making it concentration which set up the anode field and the cathode field in the above-mentioned operation gestalt. Consequently, it becomes possible to protect the gate oxide of a latter component from a surge.
[0054] moreover, low — since the substrate [****] is used, charge can be efficiently missed to GND level, the effectiveness of reducing the amount of charges impressed to a latter component is acquired, and the semiconductor device which can be contributed to improvement in a static protection function can be offered.
[0055] Furthermore, since the function of a protection component is raised compared with the conventional semiconductor device, area of the protection component itself can be made small. Moreover, it is not only possible to make transistor size small, but in an output circuit, high-speed I/O is easily realizable, since it becomes unnecessary to give big parasitic capacitance to an output transistor with low capacity-ization of an output pin. Also in an input circuit, it is also possible to realize a static protection function only for diode, without performing concomitant use with gate control mold diode which was explained with the operation gestalt. Therefore, the semiconductor device in which high integration and high-performance-izing are possible can be offered.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing the structure of the 1st operation gestalt of the semiconductor device concerning this invention.
[Drawing 2] It is the sectional view showing the production process of the semiconductor device shown in drawing 1 .
[Drawing 3] It is the circuit diagram of 1 operation gestalt which applied the semiconductor device concerning this invention to the input circuit.
[Drawing 4] It is the circuit diagram of 1 operation gestalt which applied the semiconductor device concerning this invention to the output circuit.
[Drawing 5] It is drawing showing 1 operation gestalt of the layout in the interior of LSI of the semiconductor device concerning this invention.
[Drawing 6] It is the sectional view showing the structure of the 2nd operation gestalt of the semiconductor device concerning this invention.
[Drawing 7] It is the sectional view showing the production process of the semiconductor device shown in drawing 6 .
[Drawing 8] It is the circuit diagram showing the conventional input-protection circuit.
[Drawing 9] It is the circuit diagram showing the conventional I/O protection network using a field transistor.
[Drawing 10] It is the sectional view showing the structure of the conventional field transistor.
[Description of Notations]
1 P+ Mold Substrate
2 P Wells
3 Boron **** Riser Field
4 Isolation Oxide Film
5 Gate Oxide
6 Gate Electrode
7 Side-Attachment-Wall Oxide Film
8 N+ Cathode Field
9 N+SD Field
10 Metal Silicide
11 Substrate Interlayer Insulation Film
12 Embedded Metal
13 Wiring Electrode
14 P+ Anode Field
20 Photoresist (PR)
21 Mask Material
22 N Type LDD Field
23 Photoresist (PR)

30 P Type Substrate
31 N+ Diffusion Layer Field
35 Low Proof-Pressure Static Protection Diode
36 Gate Control Mold Diode (P Type)
37 Gate Control Mold Diode (N Type)
40 Low Proof-Pressure Static Protection Diode
50 Input/output Terminal (PAD)
51 Low Proof-Pressure Static Protection Diode Formation Field
52 Internal Area
D Low proof-pressure static protection diode
T Internal transistor
T40, T41 Output transistor

[Translation done.]